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DATA SHEET

BITSTREAM CONVERSION

UDA1328T
Multi-channel filter DAC

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PHILIPS

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1 FEATURES

1.1 General

- 2.7 to 3.6 V power supply
- 5 V tolerant TTL compatible inputs
- Selectable control via L3 microcontroller interface or via static pin control
- Multi-channel integrated digital filter plus non-inverting Digital-to-Analog Converter (DAC)
- Supports sample frequencies between 5 and 100 kHz
- Digital silence detection (output)
- Slave mode only applications
- No analog post filtering required for DAC
- Easy application.

1.2 Multiple format input interface

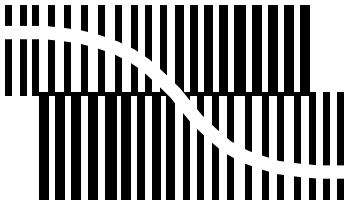
- I^2S-bus, MSB-justified and LSB-justified format compatible (in L3 mode)
- I^2S-bus and LSB-justified format compatible
- $1f_s$ input format data rate.

1.3 Multi-channel DAC

- 6-channel DAC with power on/off control
- Digital logarithmic volume control via L3; volume can be set for each of the channels individually
- Digital de-emphasis for 32, 44.1, 48 and 96 kHz f_s via L3 and, for 32, 44.1 and 48 kHz in static mode
- Soft or quick mute via L3
- Output signal polarity control via L3 microcontroller interface.

1.4 Advanced audio configuration

- 6-channel line output (under L3 volume control)
- A stereo differential output (channel 1 and channel 2) for improved performance
- High linearity, wide dynamic range, low distortion.



BITSTREAM CONVERSION

2 APPLICATIONS

This multi-channel DAC is eminently suitable for DVD like applications in which 5.1 channel encoded signals are used.

3 GENERAL DESCRIPTION

The UDA1328 is a single-chip 6-channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.

The UDA1328 supports the I^2S-bus data format with word lengths of up to 24 bits, the MSB-justified data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 18, 20 and 24 bits.

All digital sound processing features can be controlled with the L3 interface e.g. volume control, selecting digital silence type, output polarity control and mute. Also system features such as power control, digital silence detection mode and output polarity control.

Under static pin control, via static pins, the system clock can be set to either $256f_s$ or $384f_s$ support, digital de-emphasis can be set, there is digital mute and the digital input formats can also be set.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1328T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		2.7	3.3	3.6	V
V_{DDD}	digital supply voltage		2.7	3.3	3.6	V
I_{DDA}	analog supply current	6 channels active	–	28	–	mA
I_{DDD}	digital supply current		–	11	–	mA
T_{amb}	ambient temperature		–40	–	+85	°C
DAC: channels 1 and 2 differential						
$V_{o(rms)}$	output voltage (RMS value)	notes 1 and 2	–	2	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB				
		f_s = 48 kHz	–	–95	–88	dB
		f_s = 96 kHz	–	–90	–	dB
		at –60 dB; A-weighted				
		f_s = 48 kHz	–	–46	–	dB
		f_s = 96 kHz	–	–44	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted				
		f_s = 48 kHz	–	106	–	dB
		f_s = 96 kHz	–	104	–	dB
DAC: channels 3 to 6 (channels 1 and 2 non-differential)						
$V_{o(rms)}$	output voltage (RMS value)	note 1	–	1	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB				
		f_s = 48 kHz	–	–90	–83	dB
		f_s = 96 kHz	–	–85	–	dB
		at –60 dB; A-weighted				
		f_s = 48 kHz	–	–43	–	dB
		f_s = 96 kHz	–	–41	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted				
		f_s = 48 kHz	–	103	–	dB
		f_s = 96 kHz	–	101	–	dB
α_{cs}	channel separation		–	100	–	dB

Notes

1. The output voltage scales proportionally with the power supply voltage.
2. In this case the two outputs per channel (for channels 1 and 2) are combined.

6 BLOCK DIAGRAM

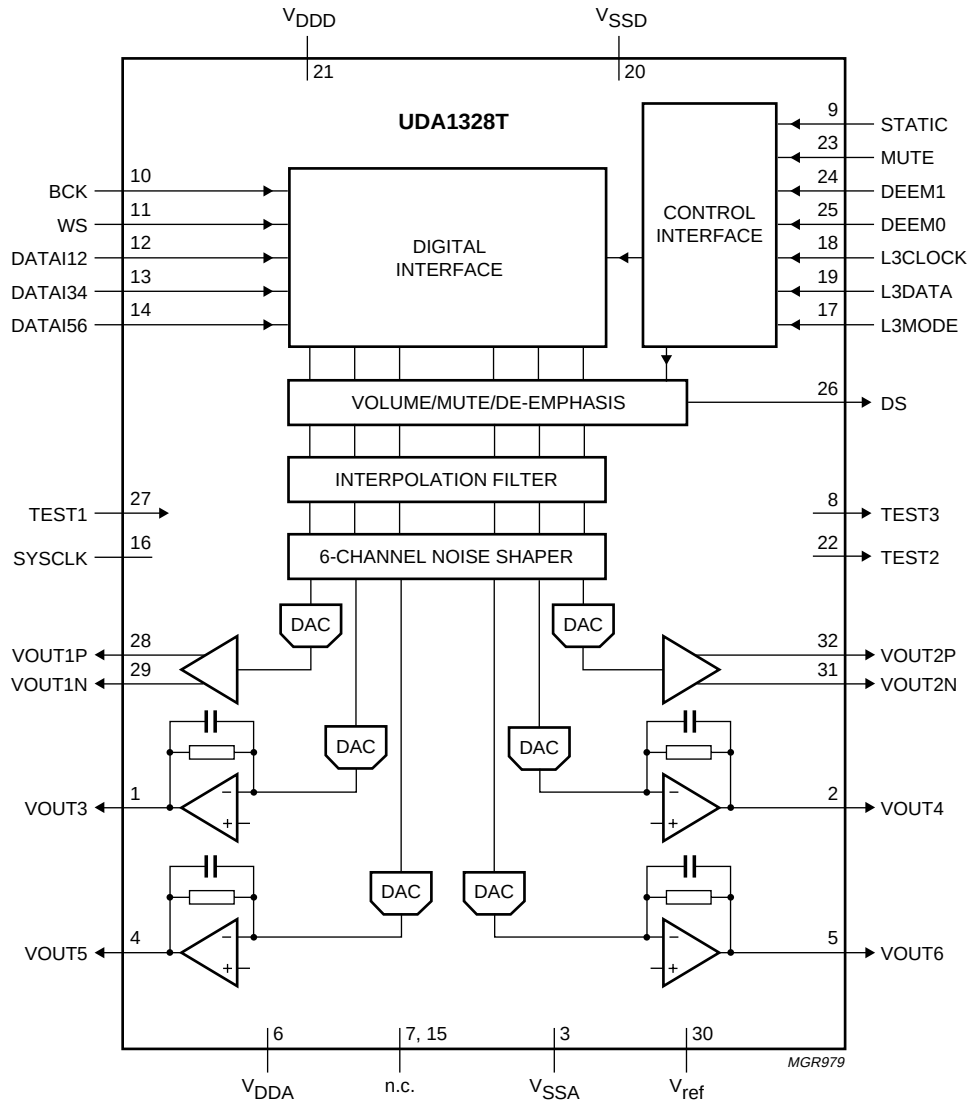


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
VOUT3	1	channel 3 analog output
VOUT4	2	channel 4 analog output
V_{SSA}	3	analog ground
VOUT5	4	channel 5 analog output
VOUT6	5	channel 6 analog output
V_{DDA}	6	analog supply voltage
n.c.	7	not connected (reserved)
TEST3	8	test output 3
STATIC	9	static mode/L3 mode switch input
BCK	10	bit clock input
WS	11	word select input
DATAI12	12	data input channel 1 and 2
DATAI34	13	data input channel 3 and 4
DATAI56	14	data input channel 5 and 6
n.c.	15	not connected (reserved)
SYSCLK	16	system clock: $256f_s$, $384f_s$, $512f_s$ and $768f_s$
L3MODE	17	L3 mode selection input
L3CLOCK	18	L3 clock input
L3DATA	19	L3 data input
V_{SSD}	20	digital ground
V_{DDD}	21	digital supply voltage
TEST2	22	test output 2
MUTE	23	static mute control input
DEEM1	24	DEEM control 1 input (static mode)
DEEM0	25	L3 address select (L3 mode)/DEEM control 0 input (static mode)
DS	26	digital silence detect output
TEST1	27	test input 1
VOUT1P	28	channel 1 analog output P
VOUT1N	29	channel 1 analog output N
V_{ref}	30	DAC reference voltage
VOUT2N	31	channel 2 analog output N
VOUT2P	32	channel 2 analog output P

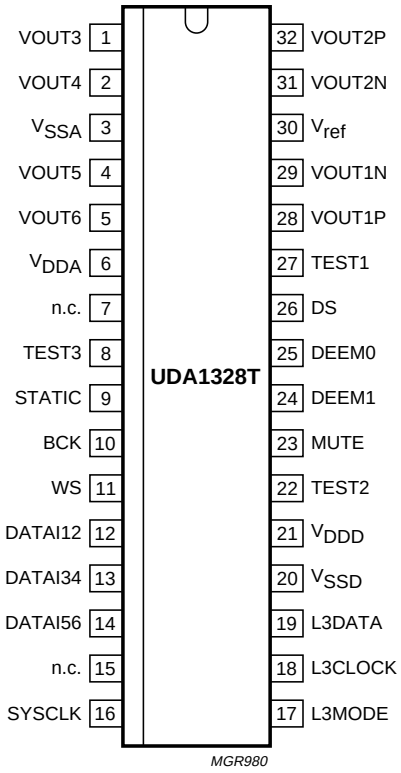


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1328 operates in slave mode only, this means that in all applications the system must provide the system clock. The system frequency is selectable. The options are $256f_s$, $384f_s$, $512f_s$ and $768f_s$ for the L3 mode and $256f_s$ or $384f_s$ for the static mode. The system clock must be frequency-locked to the digital interface signals.

It should be noted that the UDA1328 can operate from 5 to 100 kHz sampling frequency (f_s). However in $768f_s$ mode the sampling frequency must be limited to 55 kHz.

8.2 Application modes

Operating mode can be set with the STATIC pin, either to L3 mode (STATIC = LOW) or to the static mode (STATIC = HIGH). See Table 1 for pin functions in the static mode.

Table 1 Mode selection in the static mode

PIN	L3 MODE	STATIC MODE
L3CLOCK	L3CLOCK	clock select
L3MODE	L3MODE	SF1[1]
L3DATA	L3DATA	SF0[1]
MUTE	X[2]	MUTE
DEEM1	X[2]	DEEM1
DEEM0	L3ADR	DEEM0

Notes

1. SF1 and SF0 are the Serial Format inputs (2-bit).
2. X means that the pin has no function in this mode and can best be connected to ground.

8.3 Interpolation filter (DAC)

The digital filter interpolates from 1 to $128f_s$ by cascading a half-band filter and a FIR filter, see Table 2. The overall filter characteristic of the digital filters is illustrated in Fig.3, and the pass-band ripple is illustrated in Fig.4. Both figures are with a 44.1 kHz sampling frequency.

Table 2 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	±0.02
Stop band	$>0.55f_s$	–55
Dynamic range	0 to $0.45f_s$	>114
DC gain	–	–3.5

8.4 Digital silence detection

The UDA1328 can detect digital silence conditions in channels 1 to 6, and report this via the output pin DS. This function is implemented to allow for external manipulation of the audio signal in the absence of program material, such as muting or recorder control.

An active LOW output is produced at the DS pin if the channels selected via L3 or for all channels in static mode, carries all zeroes for at least 9600 consecutive audio samples (equals 200 ms for f_s = 48 kHz). The DS pin is also active LOW when the output is digitally muted either via the L3 interface or via the STATIC pin.

In static mode all channels participate in the digital silence detection. In L3 mode control each channel can be set, either to participate in the digital silence detection or not.

8.5 Noise shaper

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

8.6 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post-filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7 Static mode

The UDA1328 is set to static mode by setting the STATIC pin HIGH. The function of 6 pins of the device now get another function as can be seen in Table 1.

8.7.1 System clock setting

In static mode pin 18 (L3CLOCK) is used to select the system clock setting. When pin 18 is LOW, the device is in $256f_s$ mode, when pin 18 is HIGH the device is in $384f_s$ mode.

8.7.2 DE-EMPHASIS CONTROL

In static pin mode the pins DEEM0 and DEEM1 control the de-emphasis mode; see Table 3.

Table 3 De-emphasis control

DEEM MODE	DEEM1	DEEM0
No de-emphasis	0	0
32 kHz de-emphasis	0	1
44.1 kHz de-emphasis	1	0
48 kHz de-emphasis	1	1

8.7.3 DIGITAL INTERFACE FORMATS

In static pin mode the digital audio interface formats can be selected via pin 17 (SF1) and 19 (SF0). The following interface formats can be selected (see also Table 4):

- I^2S-bus with data word length of up to 24 bits
- LSB-justified format with data word length of 16, 20 or 24 bits.

Table 4 Input format selection in the static mode

INPUT FORMAT	SF1	SF0
I^2S-bus	0	0
LSB-justified 16 bits	0	1
LSB-justified 20 bits	1	0
LSB-justified 24 bits	1	1

It should be noted that the digital audio interface holds that the BCK frequency can be 64 times the WS maximum frequency, or $f_{BCK} \leq 64 \times f_{WS}$

8.8 L3 mode

The device is set to L3 mode by setting the STATIC pin to LOW. The device can then be controlled via the L3 microcontroller interface (see Chapter 9).

8.8.1 DIGITAL INTERFACE FORMATS

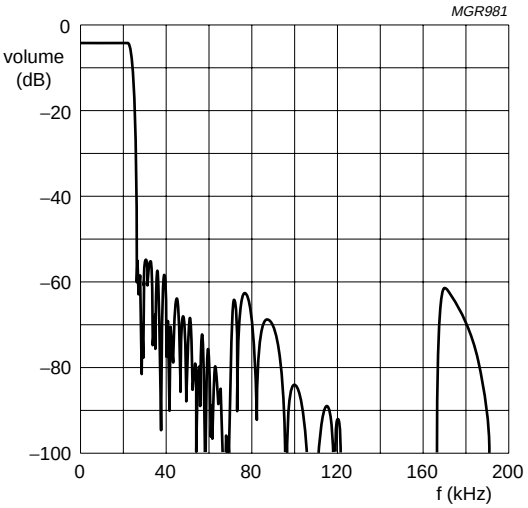
The following interface formats can be selected in the L3 mode:

- I^2S-bus with data word length of up to 24 bits
- MSB-justified with data word length of up to 24 bits
- LSB-justified format with data word length of 16, 18, 20 or 24 bits.

8.8.2 L3 ADDRESS

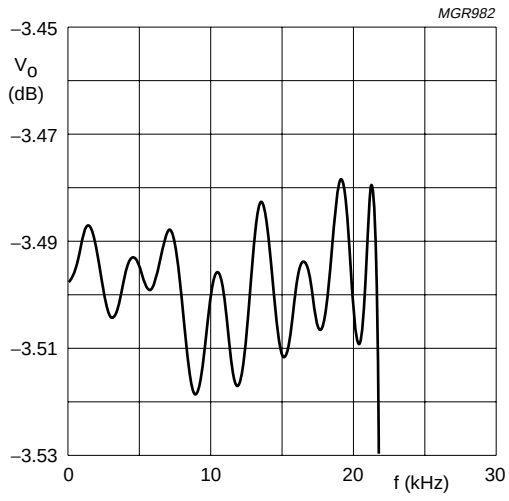
The UDA1328 can be addressed via the L3 microcontroller interface using one of two addresses. This is done in order to individually control the UDA1328 and other Philips DACs or CODECs via the same L3 bus.

The address can be selected using pin 25 (DEEM0) in L3 mode. When pin 25 is set LOW, the address is 000100. When pin 25 is set HIGH the address is 000101.



f_s = 6.14400 MHz

Fig.3 Overall frequency characteristics.



f_s = 6.14400 MHz

Fig.4 Pass-band ripple of all filters.

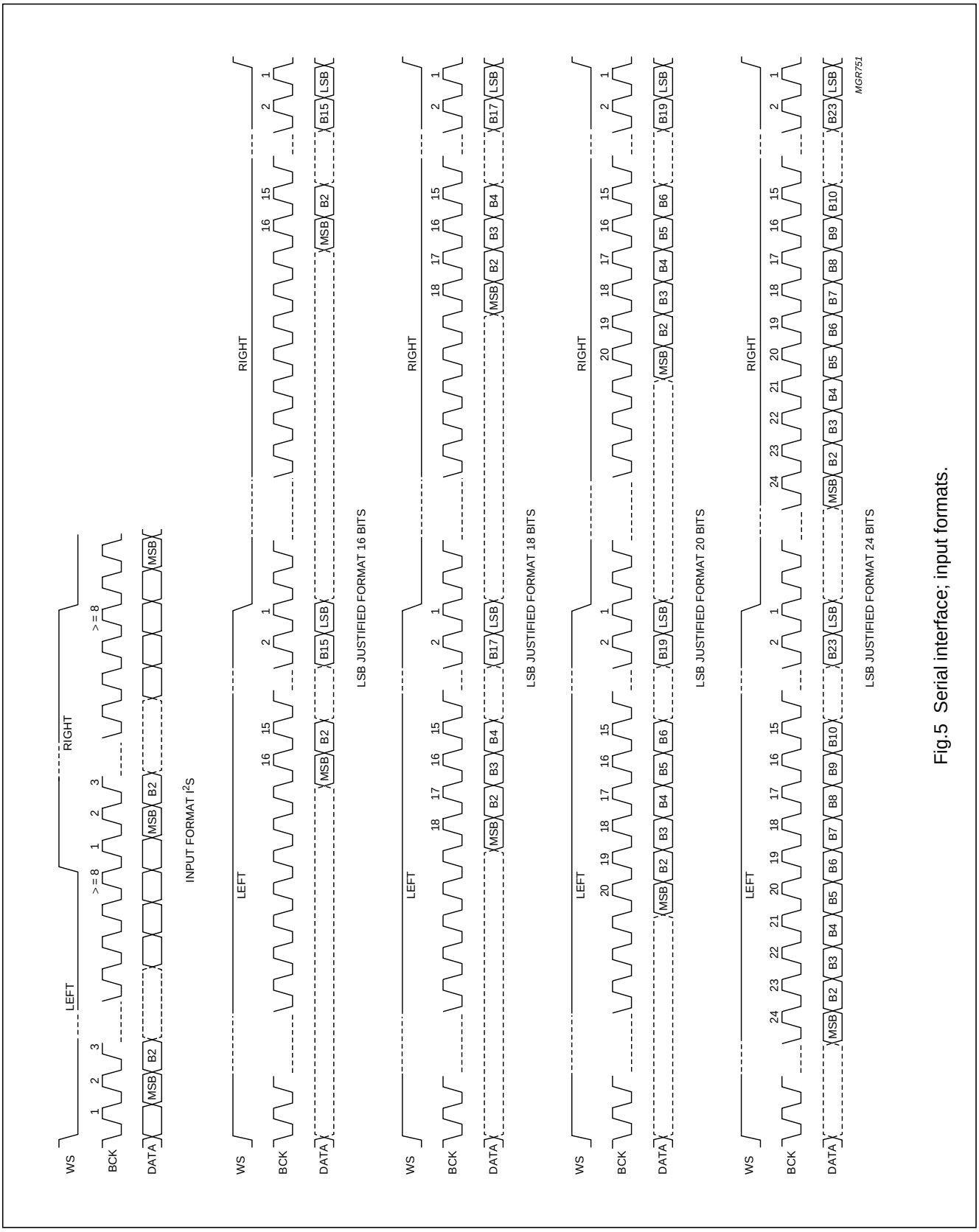


Fig.5 Serial interface; input formats.

9 L3 INTERFACE DESCRIPTION

The following system and digital sound processing features can be controlled in the microcontroller mode of the UDA1328:

- Data input format
- De-emphasis for 32, 44.1, 48 and 96 kHz
- Volume control: master and for individual channels
- Soft or quick mute: master and for individual channels
- Output polarity control: master and for individual channels
- Digital silence control: master and for individual channels
- Power-down mode.

The exchange of data and control information between the microcontroller and the UDA1328 is accomplished via a serial hardware interface comprising the following pins:

L3DATA: microcontroller interface data line

L3MODE: microcontroller interface mode line

L3CLOCK: microcontroller interface clock line.

Information transfer via the microcontroller bus is organized LSB first and is in accordance with the so called 'L3' format, in which two different modes of operation can be distinguished. The address mode and data transfer mode are illustrated in Figs 6 and 7.

The address mode is required to select a device communicating via the L3-bus and to define the destination registers for the data transfer mode. Data transfer for the UDA1328 can only be in one direction; input to the UDA1328 to program its sound processing and other functional features.

9.1 Address mode

The address mode is used to select a device for subsequent data transfer and to define the destination registers. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 data bits. The fundamental timing is shown in Fig.6. Data bits 0 and 1 indicate the type of subsequent data transfer as given in Table 5.

Table 5 Selection of data transfer

BIT 1	BIT 0	TRANSFER
0	0	data (volume, de-emphasis, mute, digital silence mode, polarity control)
0	1	not used
1	0	status (system clock frequency, data input format, mute mode, power control)
1	1	not used

Data bits 7 to 2 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the UDA1328 is 000100 (bit 7 to bit 2) when L3ADR (DEEM0) = LOW or 000101 when L3ADR = HIGH. In the event that the UDA1328 receives a different address, it will deselect its microcontroller interface logic.

9.2 Data transfer mode

The selection preformed in the address mode remains active during subsequent data transfers, until the UDA1328 receives a new address command. The fundamental timing of data transfers is essentially the same as in the address mode, shown in Fig.6. The maximum input clock and data rate is $64f_s$. All transfers are byte wise, i.e. they are based on groups of 8 bits. Data will be stored in the UDA1328 after the eighth bit of a byte has been received. A multibyte transfer is illustrated in Fig.8.

9.2.1 Programming the sound processing and other features

The sound processing and other feature values are stored in independent registers. The first selection of the registers is achieved by the choice of data type that is transferred. This is performed in the address mode, bit 1 and bit 0 (see Table 5). The second selection is performed by the 2 MSBs of the data byte (bit 7 and bit 6). The other bits in the data byte (bit 5 to bit 0) is the value that is placed in the selected registers.

When the data transfer of type 'data' is selected, the features volume, sub volume, de-emphasis, mute, digital silence settings, output polarity control and channel selection can be controlled. When the data transfer of type 'status' is selected, the features system clock frequency, data input format, mute mode and power control can be controlled.

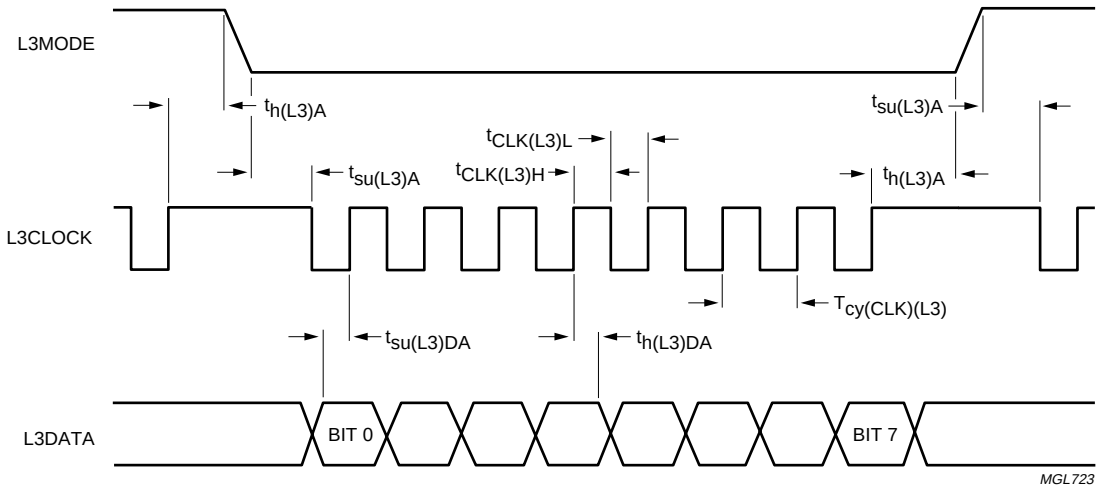


Fig.6 Timing address mode.

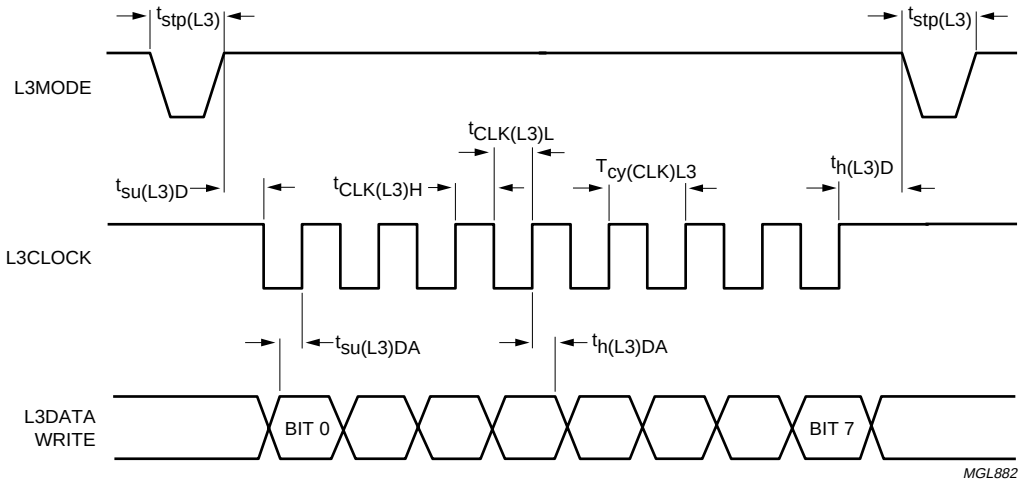


Fig.7 Timing for data transfer mode.

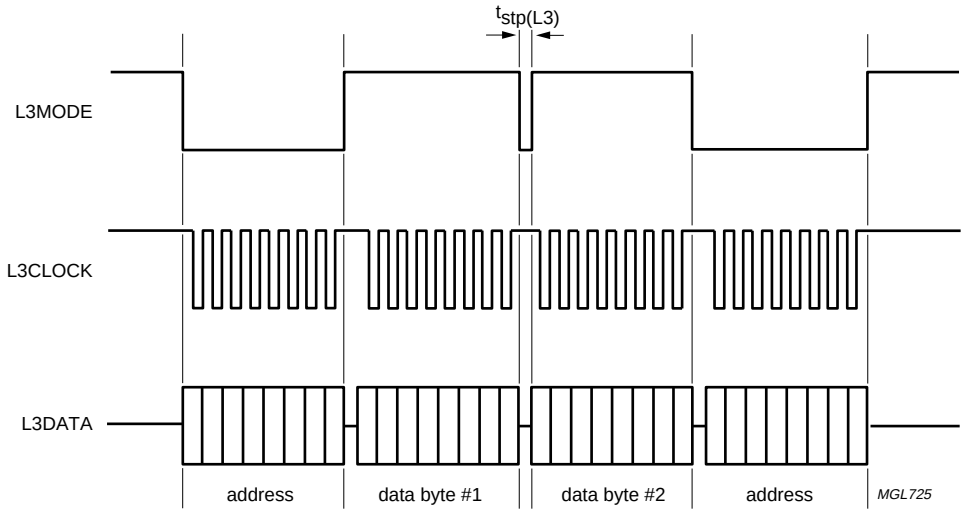


Fig.8 Multibyte transfer.

Table 6 Data transfer of type ‘status’

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	RST	SC1	SC0	IF2	IF1	IF0	0	ReSeT
								System Clock frequency (1 and 0)
								data Input Format (2 to 0)
1	0	0	0	0	0	QM	PC	Quick/soft Mute
								Power Control

Table 7 Data transfer of type ‘data’

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	VC5	VC4	VC3	VC2	VC1	VC0	Volume Control (5 to 0)
0	1	0	0	0	0	VQ1	VQ0	0.25 dB step sub volume (1 and 0)
1	0	DE2	DE1	DE0	MT	DSM	PLC	DE-emphasis (2 to 0)
								MuTe
								Digital Silence Mode
								PoLarity Control
1	1	0	0	ACH	CH2	CH1	CH0	All CHannels select
								CHannel select (2 to 0)

9.2.2 RESET BIT

A 1-bit value to initialize the L3 registers with the default settings (except the system clock setting and the data input format setting) by writing a logic 1 to RST (see Table 6).

The default settings after reset are as follows:

- Mute mode: soft mute
- Power: on
- Volume: 0 dB
- Sub volume: 0 dB
- De-emphasis: off
- Mute: off
- Silence detect mode: detect
- Polarity: non-inverting.

9.2.3 SYSTEM CLOCK FREQUENCY

A 2-bit value (SC1 and SC0) to select the used external clock frequency (see Table 8).

Table 8 System clock frequency settings

SC1	SC0	FUNCTION
0	0	$512f_s$
0	1	$384f_s$
1	0	$256f_s$
1	1	$768f_s$

9.2.4 DATA INPUT FORMAT

A 3-bit value (IF2 to IF0) to select the used data format (see Table 9).

Table 9 Data input format settings

IF2	IF1	IF0	FUNCTION
0	0	0	I^2S-bus
0	0	1	LSB-justified; 16 bits
0	1	0	LSB-justified; 18 bits
0	1	1	LSB-justified; 20 bits
1	0	0	MSB-justified
1	0	1	LSB-justified; 24 bits
1	1	0	reserved
1	1	1	reserved

9.2.5 QUICK MUTE

A 1-bit value to set the mute mode to either soft mute (via cosine roll-off), quick or hard mute.

Table 10 Quick mute

QM	FUNCTION
0	soft mute mode
1	quick mute mode

9.2.6 POWER CONTROL

A 1-bit value to disable the ADC and/or DAC to reduce power consumption.

Table 11 Power control settings

PC	FUNCTION
0	all channels off
1	all channels on

9.3 Feature settings

In the UDA1328 there are features that can be controlled either per-channel or all at the same time. These features are:

- Volume control
- Sub volume control
- Mute
- Output polarity control
- Digital silence detect.

When a ‘per-channel’ setting is required for these features, the ACH bit (see Table 7) must be set to logic 0 before writing a new value to one of the features. Once this has been performed a channel is selected via the CH2 to CH0 bits. The features for this channel can be controlled without sending the same channel address again (low microcontroller mode).

When the ACH bit is set to logic 1, which means ‘all channels select’, all channels will be set to the same value of the feature sent afterwards.

For the digital silence detector it holds that the DS pin is either active on the selected channel when bit ACH is set to logic 0 before writing the DSM bit, or the DS pin is active on all channels when the ACH bit is set to logic 1.

9.3.1 CHANNEL SELECTION MODE

A 1-bit value to set the selection mode (either individually or per-channel) for the volume, mute, polarity control and silence detect is given in Table 12. The 3-bit value is given in Table 13.

Table 12 1-bit selection

ACH[1]	FUNCTION
0	individual channel select; use CH(2 : 0)
1	all channels selected

Note

1. For setting the de-emphasis mode, the ACH bit must be set to logic 1 before setting the de-emphasis.

Table 13 3-bit selection

CH2	CH1	CH0	FUNCTION
0	0	0	channel 1 selected
0	0	1	channel 2 selected
0	1	0	channel 3 selected
0	1	1	channel 4 selected
1	0	0	channel 5 selected
1	0	1	channel 6 selected
1	1	0	not used
1	1	1	not used

9.3.2 VOLUME CONTROL

A 6-bit value to program the channel volume attenuation (VC5 to VC0). The range is 0 dB to $-\infty$ dB in steps of 1 dB (see Table 14).

Table 14 Volume settings

VC5	VC4	VC3	VC2	VC1	VC0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	–1
0	0	0	0	1	1	–2
:	:	:	:	:	:	:
1	1	1	0	1	1	–58
1	1	1	1	0	0	–59
1	1	1	1	0	1	–60
1	1	1	1	1	0	$-\infty$
1	1	1	1	1	1	$-\infty$

9.3.3 SUB VOLUME CONTROL

A 2-bit value to program the channel volume attenuation with a 0.25 dB step (VQ1 and VQ0). To validate the sub volume settings in these registers, the volume control registers of corresponding channels must be updated one after the other.

Table 15 Sub volume settings

VQ1	VQ0	VOLUME (dB)
0	0	0.00
0	1	–0.25
1	0	–0.50
1	1	–0.75

9.3.4 MUTE

A 1-bit value to enable the digital mute (the type of mute is set via the QM bit in the status register).

Table 16 Mute

MT	FUNCTION
0	no muting
1	muting

9.3.5 DIGITAL SILENCE MODE

A 1-bit value to set the digital silence mode. This bit is set together with the channel address CH2 to CH0 and the ACH bit.

When the ACH bit is set to logic 0, each channel can be selected for digital silence detection. When the ACH bit is set to logic 1 all channels are selected.

Table 17 Digital silence mode

DSM	FUNCTION
0	no participation
1	participates

9.3.6 DE-EMPHASIS

A 2-bit value to enable the digital de-emphasis filter.

Table 18 De-emphasis settings

DE2	DE1	DE0	FUNCTION
0	0	0	no de-emphasis
0	0	1	de-emphasis; 32 kHz
0	1	0	de-emphasis; 44.1 kHz
0	1	1	de-emphasis; 48 kHz
1	0	0	de-emphasis; 96 kHz

9.3.7 OUTPUT POLARITY CONTROL

A 1-bit value to program the output polarity of the output signal. This bit must be used together with the CH2 to CH0 bits and the ACH bit to either select the polarity for all channels or to set for each channel individually.

Table 19 Output polarity control

PLC	FUNCTION
0	non-inverting
1	inverting

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	–	5.0	V
V_{DDA}	analog supply voltage	note 1	–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 2	–3000	+3000	V
		note 3	–250	+250	V

Notes

1. All supply connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor, expect pin 19 (L3DATA) which can withstand ESD pulses of –2500 to +2500 V.
3. Equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor.

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

12 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	58	K/W

13 QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*. The number of the quality specification can be found in the *“Quality Reference Handbook”*.

14 DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 3.3$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ. All voltages referenced to ground (pins 3 and 20); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage	note 1	2.7	3.3	3.6	V
V_{DDD}	digital supply voltage	note 1	2.7	3.3	3.6	V
I_{DDA}	analog supply current	all channels active; operating mode	–	28	–	mA
I_{DDD}	digital supply current	operating mode	–	11	–	mA
Digital input pins: 5 V tolerant TTL compatible						
V_{IH}	HIGH-level input voltage		2.0	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
$V_{IL(th)}$	LOW-level threshold input voltage; falling edge		0.9	–	1.45	V
$V_{IH(th)}$	HIGH-level threshold input voltage; rising edge		1.4	–	1.9	V
V_{hyst}	Schmitt trigger hysteresis voltage		0.4	–	0.7	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	1	μA
C_i	input capacitance		–	–	10	pF
Digital output pin						
V_{OH}	HIGH-level output voltage	$I_{OH} = -2$ mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2$ mA	–	–	0.4	V
DAC						
V_{ref}	reference voltage	referenced to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1%	–	0.22	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	50	pF

Notes

1. All supply connections must be made to the same external power supply unit.
2. When the DAC drives a capacitive load above 50 pF, a series resistor of 100 Ω must be used to prevent oscillations in the output operational amplifier.

15 AC CHARACTERISTICS (ANALOG)

V_{DDD} = V_{DDA} = 3.3 V; f_i = 1 kHz; T_{amb} = 25 °C; R_L = 5 kΩ. All voltages referenced to ground (pins 3 and 20); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAC: channels 1 and 2 in differential mode						
$V_{o(rms)}$	output voltage (RMS value)		–	2	–	V
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_s = 48 kHz; at 0 dB	–	–95	–88	dB
		f_s = 48 kHz; at –60 dB; A-weighted	–	–46	–	dB
		f_s = 96 kHz; at 0 dB	–	–90	–	dB
		f_s = 96 kHz; at –60 dB; A-weighted	–	–44	–	dB
S/N	signal-to-noise ratio	f_s = 48 kHz; code = 0; A-weighted	–	106	–	dB
		f_s = 96 kHz; code = 0; A-weighted	–	104	–	dB
DAC: channels 3 to 6						
$V_{o(rms)}$	output voltage (RMS value)		–	1	–	V
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_s = 48 kHz; at 0 dB	–	–90	–83	dB
		f_s = 48 kHz; at –60 dB; A-weighted	–	–43	–	dB
		f_s = 96 kHz; at 0 dB	–	–85	–	dB
		f_s = 96 kHz; at –60 dB; A-weighted	–	–41	–	dB
S/N	signal-to-noise ratio	f_s = 48 kHz; code = 0; A-weighted	–	103	–	dB
		f_s = 96 kHz; code = 0; A-weighted	–	101	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 100 mV	–	50	–	dB

16 AC CHARACTERISTICS (DIGITAL)

V_{DDD} = V_{DDA} = 2.7 to 3.6 V; T_{amb} = −20 to +85 °C; R_L = 5 kΩ. All voltages referenced to ground (pins 3 and 20); unless otherwise specified. The typical timing is specified at 44.1 kHz sampling frequency.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{sys}	system clock cycle	$f_{sys} = 256f_s$	35	88	780	ns
		$f_{sys} = 384f_s$	23	59	520	ns
		$f_{sys} = 512f_s$	20	44	390	ns
		$f_{sys} = 768f_s$; note 1	20	30	260	ns
t_{CWL}	LOW-level system clock pulse width	f_{sys} < 19.2 MHz	30	–	70	$\%T_{sys}$
		$f_{sys} \geq$ 19.2 MHz	40	–	60	$\%T_{sys}$
t_{CWH}	HIGH-level system clock pulse width	f_{sys} < 19.2 MHz	30	–	70	$\%T_{sys}$
		$f_{sys} \geq$ 19.2 MHz	40	–	60	$\%T_{sys}$
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
Serial input data timing (see Fig.9)						
$T_{cy(CLK)(bit)}$	bit clock period		140	–	–	ns
$t_{CLKH(bit)}$	bit clock HIGH time		60	–	–	ns
$t_{CLKL(bit)}$	bit clock LOW time		60	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{su(i)(D)}$	data input set-up time		20	–	–	ns
$t_{h(i)(D)}$	data input hold time		0	–	–	ns
$t_{su(WS)}$	word selection set-up time		20	–	–	ns
$t_{h(WS)}$	word selection hold time		10	–	–	ns
Microcontroller interface timing (see Figs 6**,** 7 and 8)						
$T_{cy(CLK)(L3)}$	L3CLOCK time		500	–	–	ns
$t_{CLK(L3)H}$	L3CLOCK HIGH time		250	–	–	ns
$t_{CLK(L3)L}$	L3CLOCK LOW time		250	–	–	ns
$t_{su(L3)A}$	L3MODE set-up time	addressing mode	190	–	–	ns
$t_{h(L3)A}$	L3MODE hold time	addressing mode	190	–	–	ns
$t_{su(L3)D}$	L3MODE set-up time	data transfer mode	190	–	–	ns
$t_{h(L3)D}$	L3MODE hold time	data transfer mode	190	–	–	ns
$t_{su(L3)DA}$	L3DATA set-up time	data transfer and addressing mode	190	–	–	ns
$t_{h(L3)DA}$	L3DATA hold time	data transfer and addressing mode	30	–	–	ns
$t_{stp(L3)}$	L3MODE halt time		190	–	–	ns

Note

1. In the $768f_s$ clock mode, the sampling frequency must be limited to 55 kHz.

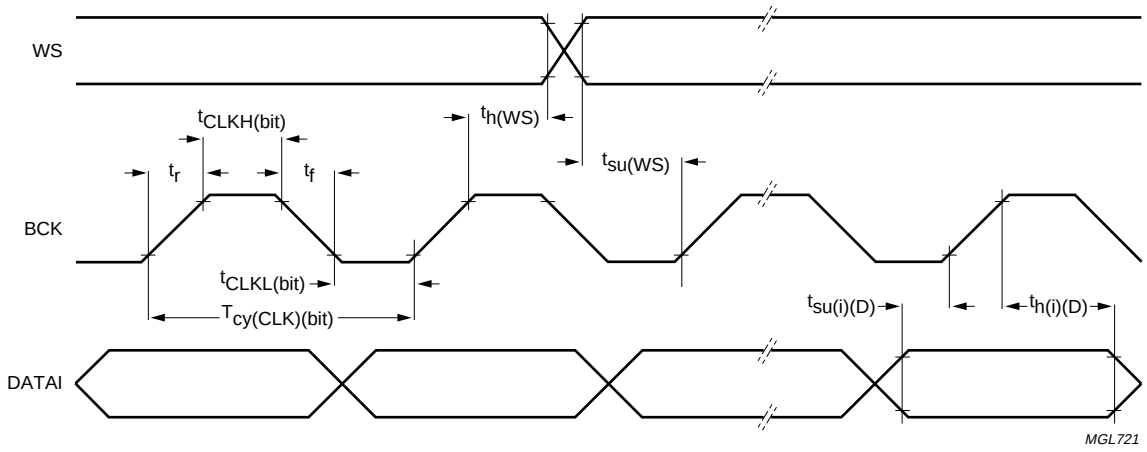


Fig.9 Serial interface timing.

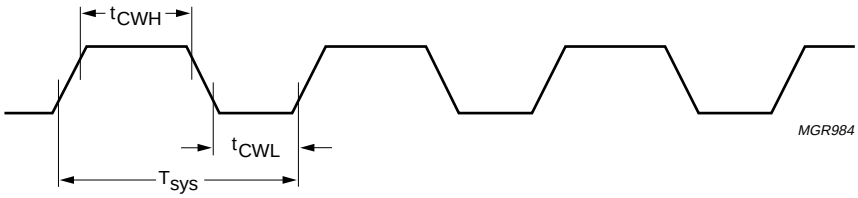


Fig.10 System clock timing.

17 APPLICATION INFORMATION

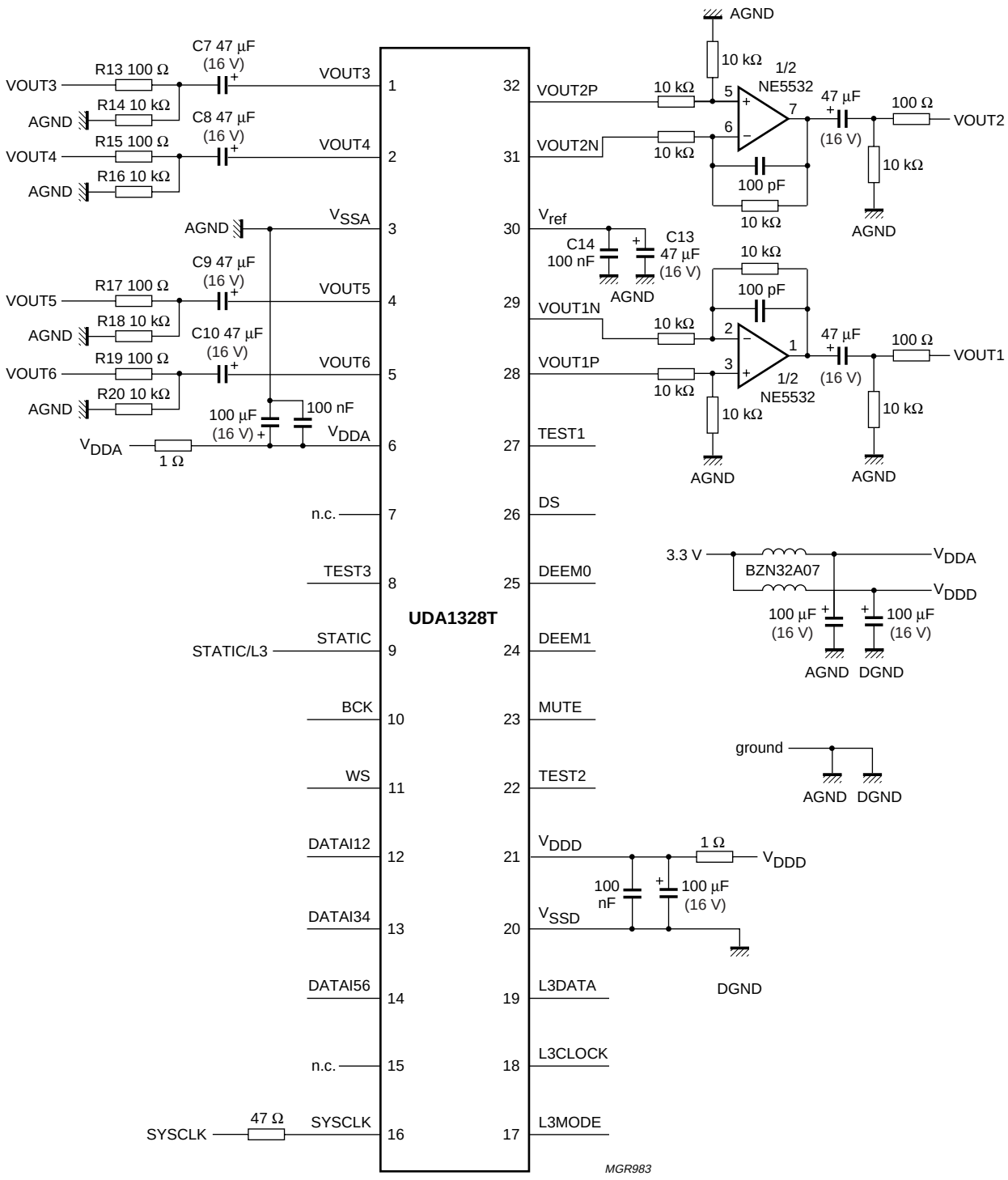
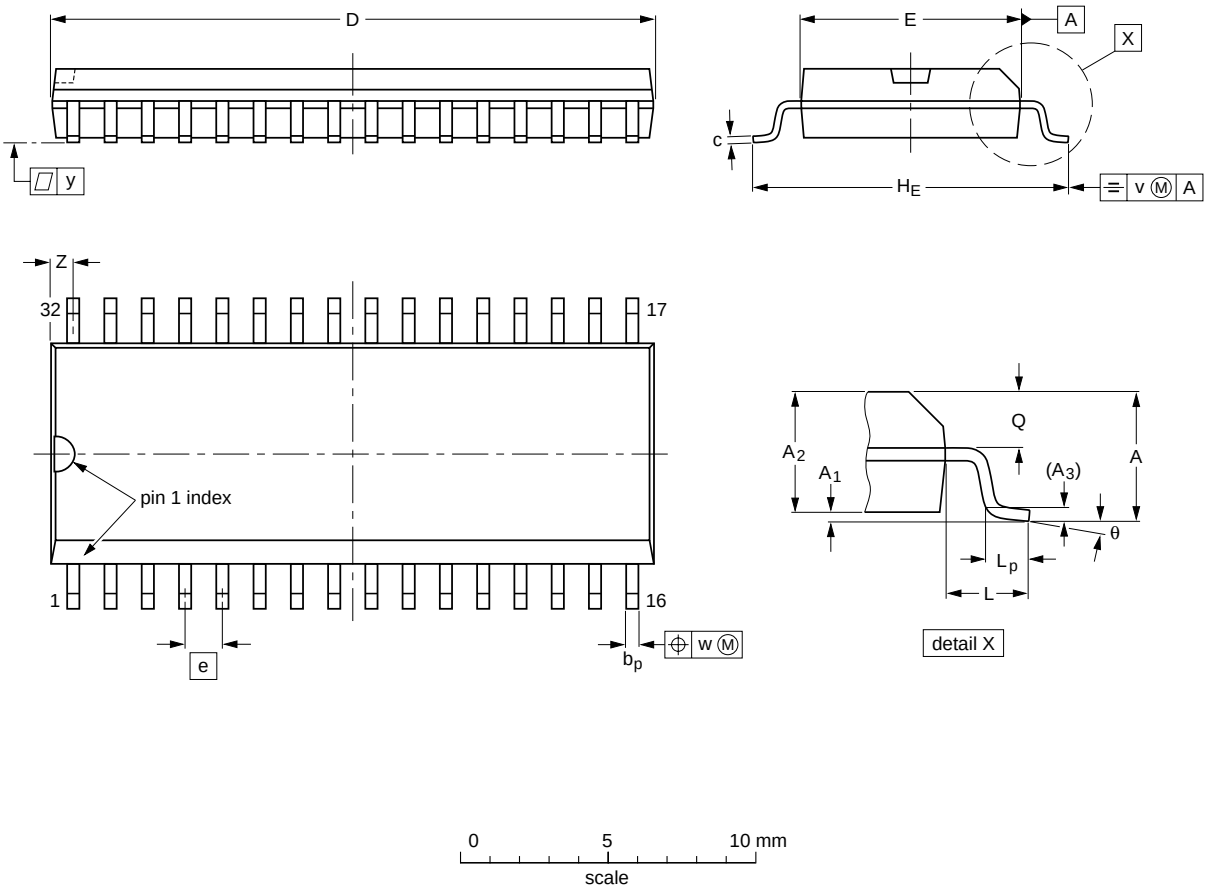


Fig.11 Application diagram.

18 PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1		MO-119				~~97-05-22~~ 99-12-27

19 SOLDERING

19.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

19.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

19.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

20 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

21 LIFE SUPPORT APPLICATIONS

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